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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,843	09/27/2000	Naoaki Komiya	YKI-0049	6716

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EXAMINER	
NGUYEN, KIMNHUNG T	
ART UNIT	PAPER NUMBER
2677	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/671,843	KOMIYA ET AL.	
	Examiner	Art Unit	
	Kimnhung Nguyen	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amentdment filed on 8/17/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application has been examined. The claims 1-15 are pending. The examination results are as following.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 6-7 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (US 6, 147,451) in view of Osada et al. (US 5,973,456).

Regarding claims 1-2, 7 and 11-12, Shibata et al. discloses in figures 2-4 that an active matrix type electroluminescence display device comprising a plurality of display pixels arranged in rows and columns in a matrix form; gate signal line (4) which is connected to and shared by a plurality of display pixels provided on each row; gate drive circuit (31) for sequentially supplying select signal to the gate signal line (4); a voltage source line is provided for each column; and voltage from a voltage source is provided from the voltage source line, wherein each of the display pixels includes an elctroluminescence element (20); a first thin film transistor (Tr1) in which a display signal is applied to the drain and which is switched on and off in response to the select signal, and a second thin film transistor (Tr2) for driving the electroluminescence element (20) based on the display signal; and the gate drive circuits (31) are placed so that said select signals are supplied from both ends of gate signal lines to said gate

signal lines, each of said gate signal lines is connected to the gate drive circuits (31) at both ends of said gate signal lines to the gate signal line (see figures 2-4, column 4, lines 14-32), and the gate drive circuits (31) include a first and second gate drive circuits arranged in a symmetric pattern to the right and left of the display portion.

However, Shibata does not disclose a voltage from a voltage source is provided to each of the columns from only on end of the voltage source line.

Osada et al. discloses in fig. 1, an EL display having a voltage from a voltage source (7) is provided to each of the columns from only on end of the voltage source line (401, 402,403).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the using of a voltage from a voltage source is provided to each of the columns from only on end of the voltage source line as taught by Osada et al. into the system of Shibata because this would provide a direct current voltage Vm to a P-channel FET side common line of the data electrode driver circuit and supply a ground voltage to an N-channel FET source-side common line of the data electrode driver circuit of the display system.

Regarding claim 6, Shibata et al. discloses in figures 2-4, an active matrix type electroluminescence display device comprising a plurality of display pixels arranged in rows and columns in a matrix form; gate signal line (4) which is connected to and shared by a plurality of display pixels provided on each row; gate drive circuit (31) for sequentially supplying select signals to the gate signal line (4); a data line (5) is provided for each column (see an X-driver 32 for feeding a data line signal to the data lines 5); and a data signal is provided from the data line (5, see figure 3); wherein each of the display pixels includes an electroluminescence element

(20); a first thin film transistor (Tr1) in which a display signal is applied to the drain and which is switched on and off in response to the select signal, and a second thin film transistor (Tr2) for driving the electroluminescence element (20) based on the display signal; and the gate drive circuits (31) are placed so that said select signals are supplied from both ends of gate signal lines to said gate signal lines, each of said gate signal lines is connected to the gate drive circuits (31) at both ends of said gate signal lines to the gate signal line (see figures 2-4, column 4, lines 14-32).

However, Shibata et al. does not disclose a data signal is provided from only one end of the data line. Osada et al. discloses in fig. 1, an EL display having the data signal is provided from only one end of the data line.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the using of the data signal is provided from only one end of the data line as taught by Osada et al. into the system of Shibata et al. because this would provide a direct current voltage Vm to a P-channel FET side common line of the data electrode driver circuit and supply a ground voltage to an N-channel FET source-side common line of the data electrode driver circuit of the display system.

3. Claims 3, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (US patent 6,147,451) and Osada et al. (US 5,973,456) and in view of Channing et al. (US patent 4,837,566).

Shibata et al. and Osada et al. disclose the active matrix type electroluminescence display device comprising a plurality of display pixels arranged in rows and columns in a matrix form as disclosed in claims 1-2.

However, Shibata et al. and Osada et al. do not disclose each of said first and second gate drive circuits includes a plurality of shift registers for sequentially shifting a reference clock with a pulse width of one horizontal period.

Channing et al. discloses in figure 8, a drive circuit for operating an electroluminescent display comprising a plurality of shift registers (69, 71) at left and right row drivers (see figure 8, column 9, lines 3-5) and a VSYNCD pulse width of one horizontal period (see figures 8, 11, column 9, lines 3-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a plurality of shift registers at left and right row drivers and a VSYNCD pulse width of one horizontal period as taught by Channing et al. into the system having the first and second gate drive circuits of Shibata et al. and Osada et al. because this would reverse polarity of the blanking signals, and the left and right row drivers are alternately activated to sequentially scan the rows of the matrix of the display system (see column 9, lines 21-27).

4. Claims 4-5, 9-10 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (US patent 6,147,451) in view of Osada et al. (US 5,973,456) and in view of Chaning et al. (US patent 4,837,566) as applied to claim 1 above, and further in view of Mihara (US patent 6,421,034).

Shibata et al. and Osada et al. disclose the active matrix type electroluminescence display device comprising a plurality of display pixels arranged in rows and columns in a matrix form as disclosed in claims 1-2. Channing et al. discloses in figure 8, a drive circuit for operating an electroluminescent display comprising a plurality of shift registers (69, 71) at left and right row drivers.

However, Shibata et al., Osada et al. and channing do not disclose each of the first and second gate drive circuits includes buffer amplifiers for driving said gate signal lines based on the output of registers and corresponds to the number of rows of said plurality of display pixels.

Mihara discloses in figure 1, an EL driver circuit having a plurality of amplifiers (OP1, OP2, OP3, OP4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the using of a plurality of amplifiers as taught by Mihara into the first and the second gate drive circuits corresponds to the number of rows of the plurality of display pixels of Shibata et al., Osada et al. and Channing et al.'s system because this would provide the amplifying voltage, current or power in the system display.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimnhung Nguyen
October 27, 2005

AMR A. AWAD
PRIMARY EXAMINER